CLAIMS

1. A memory controller, comprising:
at least one bus interface, each bus interface being for connection to at least one respective devices for receiving memory access requests;
a memory interface, for connection to a memory device; and
control logic, for placing received memory access requests into a queue of memory access requests,
wherein, when a memory access request is a read access request which requires multiple bursts of data to be read from the memory device, the control logic calculates the number of required data bursts and a starting address for each burst, and places the respective memory access requests into the queue of memory access requests such that back-to-back SDRAM read bursts can be performed.

2. A memory controller as claimed in claim 1, wherein, when a memory access request is a read access request which requires multiple bursts of data to be read from the memory device, the calculated starting address for a first of said required data bursts comprises a row address and a column address, and the calculated starting address for a second and any subsequent required data bursts comprises a column address but no row address.

3. A memory controller as claimed in claim 2, wherein the calculated starting address for the first of said required data bursts further comprises a chip select indication.

4. A memory controller as claimed in claim 1, comprising a plurality of bus interfaces, wherein memory access requests received from different bus interfaces may be placed into the queue of memory access requests with different priorities.

5. A memory controller as claimed in claim 1, comprising a plurality of bus interfaces, wherein memory access requests received from different bus interfaces may be placed into the queue of memory access requests with priorities determined in such a way as to maximise efficient usage of a memory bus connected to the memory interface.

6. In a memory controller, comprising at least one bus interface, each bus interface being for connection to at least one respective devices for receiving memory access requests; and a memory interface, for connection to a memory device; the method comprising:
when a memory access request is a read access request which requires multiple bursts of data to be read from the memory device, calculating the number of required data bursts and a starting address for each burst, and
placing the respective memory access requests into a queue of memory access requests such that back-to-back SDRAM read bursts can be performed.

7. A method as claimed in claim 6, comprising, when a memory access request is a read access request which requires multiple bursts of data to be read from the memory device, calculating said starting address for a first of said required data bursts comprising a row address and a column address, and calculating said starting address for a second and any subsequent required data bursts comprising a column address but no row address.

8. A method as claimed in claim 7, comprising calculating said starting address for the first of said required data bursts comprising a chip select indication.

9. A method as claimed in claim 6, in a memory controller comprising a plurality of bus interfaces, comprising

placing memory access requests received from different bus interfaces into the queue of memory access requests with different priorities.

10. A method as claimed in claim 6, in a memory controller comprising a plurality of bus interfaces, comprising placing memory access requests received from different bus interfaces into the queue of memory access requests with priorities determined in such a way as to maximise efficient usage of a memory bus connected to the memory interface.

11. A memory controller, comprising:

at least one first bus interface, for connection to a master device for receiving memory access requests and for transmitting data to the master device;

a second bus interface, for connection to a memory device, such that data can be retrieved from the memory device in data bursts;

control logic, for receiving memory access requests from the or each first bus interface, and for calculating a required number of data bursts needed to deal with each received memory access request; and

a queue store, for storing data relating to required data bursts,

wherein the control logic stores data in the queue store, relating to each of the required number of data bursts.

12. A memory controller as claimed in claim 11, wherein the control logic stores data in the queue store, relating to each of the required number of data bursts, such that the data bursts corresponding to a received memory access request can be retrieved without incurring a separate read latency for each data burst.

13. A memory controller as claimed in claim 11, wherein the control logic stores data in the queue store, indicating that the required number of data bursts correspond to a single received memory access request.